

# 國立交通大學試題紙

科目：計算機結構 (A)

日期：96 年 7 月 26 日 第 1 頁 共 3 頁

請 “✓” 明    ✓不可看書    可看書

\* 請將答案依題號順序寫入答冊

1. (5 %)

- (a) What is instruction-level parallelism?
- (b) Give three factors which will limit the instruction-level parallelism?

2. (25 %)

For the following problem, assume an in-order DLX-style pipelined architecture that has functional units that take the following number of execution cycles:

- 1. Floating-point multiplier: **4 cycles**
- 2. Floating-point adder: **2 cycles**
- 3. Integer operations: **1 cycle**

Assume as well there is **one branch delay slot**, that there is no delay between integer operations and dependent branch instructions, and that the load-use latency is **2 cycles** (i.e. **2 cycles** needed to use the data after load a data). Assume that all functional units are fully pipelined and bypassed. The following code computes a dot product. Assume that `r1` and `r2` contain addresses of arrays of floating-point numbers, and `r3` contains the length of the arrays (in elements). Assume that `r4` is initialized to zero. Then, the dot product can be computed as follows:

```
loop:  ld    f5, 0(r1)    ; load element from first array
      ld    f6, 0(r2)    ; load element from second array
      multd f7, f5, f6    ; multiply elements
      addd  f4, f4, f7    ; add elements to accumulator in f4
      addi  r1, r1, #8    ; increment pointers
      addi  r2, r2, #8
      subi  r3, r3, #1    ; decrement element count
      bnez  r3, loop      ; continue until all elements done
      nop                ; (branch delay slot)
```

(a) How many cycles does this loop take per iteration? Indicate stalls in the above code by labeling each of them with a number of cycles of stall:

(b) Reschedule this code to run with as few cycles per iteration as possible. Do not unroll it or software pipeline it. How many cycles do you get per iteration of the loop now?

(c) Unroll the loop once and schedule it to run with as few cycles as possible per iteration of the original loop. How many cycles do you get per iteration now?

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(d) If you were to unroll the loop 8 times, how many cycles per iteration would this achieve? (*hint: you do not need to actually perform the unrolling to answer this question*)

(e) Software pipeline the given loop so that it has **three iterations** overlapped simultaneously, and so that it has **no stalls**. Give the code for your solution below. Do not show start-up or clean-up code.

3. (14 %)

(a) How long would the following instructions take to **execute** on a double issue in-order superscalar processor with two execution units, where each execution unit can execute any operation, load operations have a latency of 3 cycles, and all other operation have a latency of 2 cycles? Please using detail timing of instruction issue sequence to show your answer. Assume the processor has a 5-stage pipeline.

(b) How long would the following instructions take to **issue** on a double issue out-of-order superscalar processor with two execution units, where all operation latencies are the same as above? Please using detail timing of instruction issue sequence to show your answer. Use the greedy scheduling assumption.

```
LD r4, (r5)
LD r7, (r8)
ADD r9, r4, r7
LD r10, (r11)
MUL r12, r13, r14
SUB r2, r3, r1
ST (r2), r15
MUL r21, r4, r7
ST (r22), r23
ST (r24), r21
```

4. (6 %)

Use the following code sequence for a DLX-like ISA with **no** branch delay slot. This sequence contains 3 branches, labeled by **PC1**, **PC2**, and **PC3**. The followings are the snapshot of taken/not-taken patterns for each of these branches (**T** indicates taken, **N** indicates not taken):

**PC1:** T N T T N T

**PC2:** T T T T T N

**PC3:** T T T T T T

Assume that an (1, 1) predictor is used as the prediction algorithm for predicting the execution of the three branches in this loop. What is the prediction success rate (that is, the ratio of correctly predicted branches to total branches of the snapshot) for each of the three branches (**PC1**, **PC2**, and **PC3**)? Assume that all predictors initialized to **N**.

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```

        addi r2, r0, #45      ; initialize r2 to 101101, binary
        addi r3, r0, #6       ; initialize r3 to 6, decimal
        addi r4, r0, #10000   ; initialize r4 to a big number
top:     andi r1, r2, #1       ; extract the low-order bit of r2
PC1-->  bnez r1, skip1        ; branch if the bit is set
        xor  r0, r0, r0       ; dummy instruction
        skip1: srli r2, r2, #1 ; shift the pattern in r2
        subi r3, r3, #1       ; decrement r3
PC2-->  bnez r3, skip2
        addi r2, r0, #45      ; reinitialize pattern
        addi r3, r0, #6
        skip2: subi r4, r4, #1 ; decrement loop counter
PC3-->  bnez r4, top
```