國 立 交 通 大 學 試 題 紙

一百零八學年度第二學期
博士班資格考

科目:計算機架構 A　　日期: 109年 7 月 14 日　第 1 頁 共 2 頁

請" ✓" 明　　✓不可看書　　可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

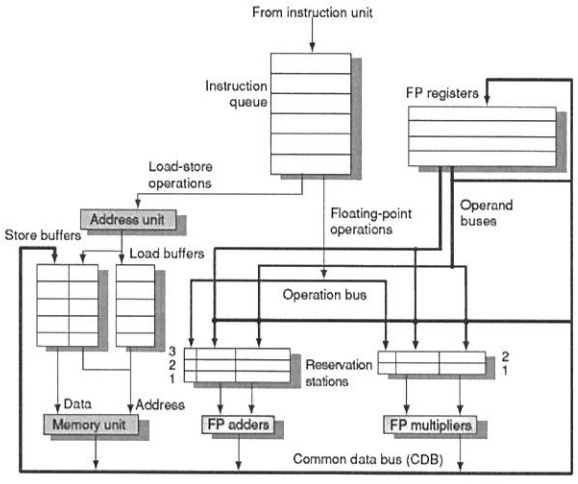
1. (6%) Describe the characteristics, one main advantage and one main disadvantage for each of the following three architectures: ***stack***, ***accumulator***, and ***general-purpose-register*** architectures.

2. (6%) Describe the characteristics, one main advantage and one main disadvantage for each of the following three techniques for evaluating branch conditions: ***condition code***, ***condition register***, and ***compare and branch***.

3. (8%) Give the equation to calculate the CPI (clocks per instruction) for a pipelined processor,
   Pipeline CPI = Ideal pipeline CPI + Structural stalls + Data hazard stalls + Control stalls
   For each of the following techniques, describe its basic idea and indicate which ones of the components of the CPI equation does the technique affect? If a technique affects data hazard stalls, please specify the dependence types (true, anti, and/or output dependences) of the hazards.
   (a) Forwarding and bypassing　　(b) Dynamic branch prediction
   (c) Multiple issue　　(d) Function unit pipelining

4. (8%)
   (a) Describe the characteristics of a pipeline-fashioned RISC datapath while comparing with an unpipelined one.
   (b) Describe the characteristics of ***simultaneous multithreading*** and the hardware mechanisms required for it.

5. (10%) Give the basic structure of **Tomasulo algorithm**.
   (a) Describe the key idea of this algorithm and the purposes of using ***reservation stations*** in this structure.
   (b) Describe the following three steps of the algorithm: ***Issue***, ***Execute***, and ***Write result***.
   (c) Describe the key idea and additional hardware required for the extension of this algorithm to support ***speculation***.



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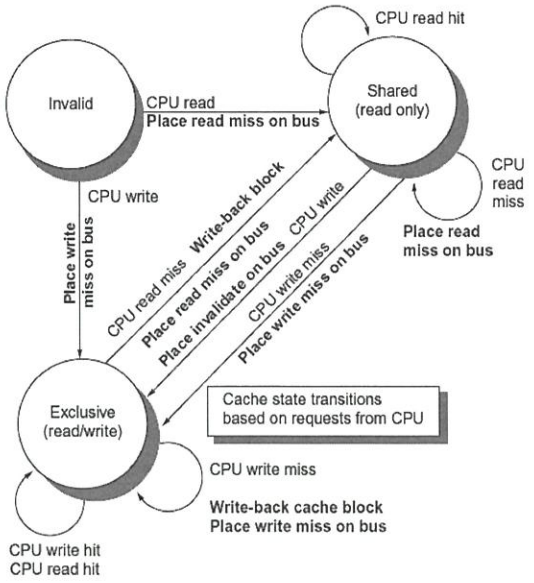
6. (6%) Describe the two methods, ***write-invalidate*** and ***write update***, for maintaining the cache coherence requirement. And, compare these two protocols in the following four aspects: (i) multiple writes to the same word with no intervening reads, (ii) with multiword cache block, (iii) delay between writing a word in one processor and reading the value in another processor, and (iv) bus and memory traffic.

7. (6%)
   (a) Describe the technique using by the ***snooping*** cache coherence protocol to track the sharing status of a data block.
   (b) Given the cache state transition subdiagram based on the requests from CPU for a single private cache block using a ***write invalidation snooping protocol*** and a ***write-back cache***, draw the cache state transition subdiagram based on the requests from bus for a cache block. (Hint: The four possible requests from CPU are *CPU read hit*, *CPU read miss*, *CPU write hit*, and *CPU write miss*. The three possible requests from bus are *Read miss for the block*, *Write miss for the block*, and *invalidate for the block*.)



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