

科目：計算機架構 A

日期：102 年 1 月 30 日 第 1 頁 共 2 頁

請“✓”明 ✓不可看書 可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (15%) ILP (instruction-level parallelism) can be exploited within only limited areas of a program.
 - (a) (3%) How do we usually call such a code area? What special feature(s) define (or indicate) such an area?
 - (b) (4%) Is it desired that such areas be enlarged or shrunk (縮小) for exploiting more ILP? And why do you say so?
 - (c) (8%) What are the well-known techniques to deal with the desire in (b)? Name one hardware technique and one software technique, and give sufficient explanation to each of the two.
2. (11%) Multi-core design has been the trend in the past decade, and we are going to see if it does have advantage in energy efficiency, in addition to the obvious performance advantage. Use a fully parallelizable program as an example, and given that $P_{dynamic} = \frac{1}{2} \times C_{load} \times V^2 \times f_{clock}$, $P_{leakage} = 0$, and $f \propto V$ (ignoring that the latter two equations are over-simplified).
 - (a) (3%) How much energy is used if we run this program on only one core? Make necessary assumption(s).
 - (b) (5%) How much energy is used if we run this program on two cores using the same amount of time as in (a)? Assume that the two cores you use here are the same as that in (a).
 - (c) (3%) For case (b), is it possible that we use simpler and more power/energy-efficient cores to achieve the same speed? Support your answer, and make any reasonable assumptions as you like.
3. (12%) Given a computer whose load/store instructions use 32-bit effective addresses, and each such address location contains 8 bits.
 - (a) (3%) What is the virtual address space of this computer?
 - (b) (3%) The physical memory is byte-addressable whose size is 1 GB. What is the size of a physical address?
 - (c) (3%) The plain page table contains 512k entries. What is the page size?
 - (d) (3%) How many bits do we need in order to specify a page? And how many page frames can we have in the main memory?
4. (12%) Continued with all the applicable information in 3. above:
 - (a) (3%) Let the L1 cache be virtual, placement be 2-way set-associative, way size be 256, and block size be 32B. Use a picture to show how the address sent to access L1 cache is partitioned into what fields, each of what size.

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- (b) (3%) Continued from (a) above, and further assume that the cache is unified (meaning it stores both code and data) and uses LRU replacement. Use a picture to show how an L1 cache block contains what fields, each of what size.
- (c) (3%) Let the L2 cache be physical, placement be 16-way, way size be 1024, and block size be 128B. Use a picture to show how the address sent to access L2 cache is partitioned into what fields, each of what size.
- (d) (3%) Continued from (c) above, and further assume that the cache unified, uses LRU replacement (although this is unlikely), and each block is further divided into 2 sub-blocks which can fetched into L2 on-demand independently. Use a picture to show how an L2 cache block contains what fields, each of what size.

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國立交通大學試題紙

一百零一學年度第一次
博士班資格考

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1. (8%)

- (a) (4%) Describe or draw the block diagram to show the operand locations of the following four different instruction set architectures: Stack architecture, Accumulator architecture, Register-memory architecture, and Register-register (Load-store) architecture.
- (b) (4%) Describe the four properties of instruction set which may help compiler writer to design a compiler that will generate efficient and correct code.

2. (10%)

- (a) (2%) Describe Amdahl's Law and define the equation of the overall speedup of an enhanced mode with respect to the original machine.
- (b) (8%) Assume a disk subsystem with the following components and MTTF (mean time to failure):

| Component | No. of components | MTTF (hours) |
|-----------------|-------------------|--------------|
| Disk | 8 | 1,000,000 |
| SCSI controller | 1 | 500,000 |
| Power supply | 1 | 200,000 |
| Fan | 1 | 200,000 |

The lifetimes of the components are exponentially distributed and the failures are independent.

- i. (3%) Compute the failure rate in FIT (failures in time, i.e., failures per billion hours of operation) and the reliability, i.e., the MTTF, of the system.
- ii. (3%) Assume that one fan is sufficient to cool the disk subsystem, one redundant fan is added to the subsystem, and the repair time of a fan is 20 hours. Calculate the failure rate and the reliability of the fan pair. And how much is it more reliable than a single fan?
- iii. (2%) Calculate the reliability improvement of the whole disk subsystem with a redundant fan by applying Amdahl's Law.

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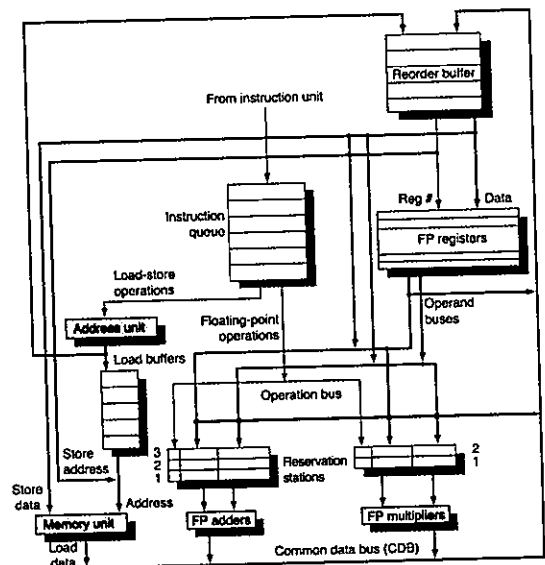
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3. (8%) For a 4-GHz processor, the instruction mix and the clock cycle count per instruction for different instruction types of a program and the processor, respectively, are given below. Assume that the total number of instructions executed is 8,000,000.

| Instruction type | Instruction mix | Clock cycle count per instruction |
|--------------------|-----------------|-----------------------------------|
| Integer ALU ops | 40% | 1 |
| Floating-point ops | 25% | 6 |
| Loads & Stores | 20% | 4 |
| Branches | 15% | 2 |

- (a) (4%) Determine the effective CPI and execution time for this program.
- (b) (4%) Assume that we build an optimizing compiler to discard 50% of the load/store instructions from the original instruction mix, determine the effective CPI of the enhancement and the speedup of the enhancement to the original design.
4. (12%)
- (a) (3%) Define "Data Hazard", "Control Hazard", and "Structure Hazard."
- (b) (3%) For data hazards involving registers, three forms exist: RAW (read after write), WAR, and WAW. Describe briefly two possible ways to avoid each of these hazards.
- (c) (3%) Describe the following schemes of dynamic branch prediction: 1-bit prediction, 2-bit prediction, and correlating branch prediction.
- (d) (3%) Describe the goal of loop unrolling and two of the major decisions or transformations made for obtaining the final unrolled code of a loop.
5. (6%) Given the structures of Tomasulo algorithm with reorder buffer (ROB) to handle speculation,
- (a) (2%) Describe two key ideas of this Tomasulo algorithm.
- (b) (4%) Describe the following four stages of the algorithm: Issue, Execute, Write result, Commit.



6. (6%) Describe the characteristics, one major advantage, and one major disadvantage for each of a VLIW (very long instruction word) processor and a dynamically scheduled superscalar processor.

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