國立交通大學試題紙

九十九學年度第二次
博士班資格考

科目：計算機結構(A)　　日期： 100 年 7 月 27 日　第 1 頁 共 2 頁

請 "✓" 明　✓不可看書　可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. **(15 points)** True or False. You need to justify your answer to receive full points:
   (a) MIPS rating is a poor measure of performance because it completely ignores the effects of clock cycle time.
   (b) Cache miss is handled by hardware.
   (c) In our 5-stage pipelined implementation, forwarding can resolve all types of data hazard.
   (d) Increasing cache line (block) size reduces capacity misses.
   (e) Increased pipelining improves clock frequency but does not change IPC (instructions per cycle).

2. **(15 points)** Short answer.
   (a) What is the goal of the memory hierarchy?
   (b) The memory hierarchy works because of what two principles?
   (c) What is the difference between a write-back cache and a write-thru cache? What is one advantage of a write-back cache? What is one advantage of a write-thru cache?
   (d) (3 points) What is a write buffer? Does a write buffer have a bigger performance impact on a system that uses a write-back cache or one that uses a write-thru cache? Why?
   (e) Calculate the page table size in bits for the following process: 32-bit byte-addressable virtual address space, 1 kB page size, and every page table entry has 10 bits for valid, replacement, protection, etc.

3. **(6 points)** If an unpipelined processor with a cycle time of 30 ns,
   (a) is evenly divided into 5 pipeline stages using pipeline latches with 1 ns latency, what is cycle time and total latency of the resulting pipeline processor?
   (b) is divided into 5 pipeline stages with latencies 5, 7, 3, 7, and 8 ns, if the pipeline latches is 1 ns, what is cycle time and total latency of the resulting pipeline processor?

4. **(14 points)** The function bzero(void *b, size_t len) writes 0 to the string b by the amount of len bytes. If len is 0, bzero() does nothing. The following MIPS assembly code implements bzero() that clears bytes one by one:

```
bzero:  beq $a1, $zero, end
loop:   store $zero, 0($a0)
        add $a0, $a0, 1
        sub $a1, $a1, 1
        bne $a1, $zero, loop
end:    jr $ra
```

Suppose you want to run bzero() to clear a string of 20 bytes on a 4 GHz processor with the following CPI table.

Instruction type	CPI
Arithmetic (add, sub)	3
Data transfer (load, store)	5
Control (branch, jump)	4

(a) (5 points) How much CPU time does it take?
(b) (5 points) What is the average CPI?
(c) (4 points) If you could reduce the CPI of one instruction type (arithmetic, memory, or control) by a single cycle, which instruction type would be the best choice and why?

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答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. **(20 points)** If processor time is given by $\frac{instructions}{program} \times \frac{cycles}{instruction} \times \frac{time}{cycle}$, discuss the effects of the following design changes for the three terms and briefly explain your answers. (You may use 0 (no-affect), + (increase), and - (decrease) to indicate the effect and be sure to explain your observation. You may answer them in a tabular form.) Also please briefly give impacts on hardware complexity.
   (a) Superscalar→VLIW
   (b) A 4-stage pipelining →8-stage pipelining
   (c) without →with loop unrolling/software pipelining
   (d) static instruction scheduling →dynamic scheduling with reorder buffer

2. **(15 points)** Instruction Level Parallelism (ILP)
   (a) What does ILP refer in the design of a CPU? How is related to IPC (instruction per cycle)?
   (b) (3 points each) Briefly explain how the following techniques can improve the ILP. Also give possible side effects or cost by the techniques.
      1) Branch prediction
      2) Simultaneously multithreading (SMT)
      3) Register renaming
      4) Speculative execution

3. **(15 points)** In contemporary processors, the CPU only shares 1/4 of the whole chip area. Please propose at least three possible approaches to take advantages of the rest of area for improving the processor performance. Why and how? For each your solution, please give what side effects your solutions may generate. (Do not limit your discussion just on large register file or caches. Your answers will be graded by the soundness, creativity, and feasibility of your solutions.)