

科目：計算機架構 A

日期：103 年 1 月 22 日 第 1 頁 共 1 頁

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* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (16%) In computer architecture for general-purpose computing,
 - (a) What does the so-called load-store architecture mean? What does the so-called register-register architecture mean? And are they dependent or independent?
 - (b) Addressing modes are used to specify the address of a memory object, or sometimes even the object itself. Let the memory object of interest be an instruction. What addressing mode(s) are typically used? Also, specify the occasion(s) in which each addressing mode in your answer is used. Note: 1. Avoid any unusual case, and 2. Only listing addressing mode(s) without explanation to its use will earn you no credit.
 - (c) How many kinds of control flow instructions are there in typical ISA designs? Give the type name, explanation and example to each kind.
 - (d) Data types include word, double-/half-word, byte, bit, etc. For data movement type instructions, do we need to specify the data type? Why? And then repeat this question for data processing type instructions.
2. (12%) Pipelining is a fundamental technique in taking advantage of instruction-level parallelism. Let us talk about a basic, single pipeline now:
 - (a) (3%) What are the five pipeline stages used extensively in our reference text? List them in order of occurrence, and briefly state what tasks should be performed in each stage.
 - (b) (2%) If we do data forwarding, in what case (i.e., for what data producing instructions) can there be no pipeline stall cycle at all? Support your answer.
 - (c) (2%) Continued from (b), in what case (i.e., for what data producing instructions) must there be pipeline stall cycle(s)? Also support your answer.
 - (d) (5%) There may also be structural hazards which may introduce pipeline stall cycles, but fortunately we can easily eliminate these all. For each of the five pipeline stages, point out one possibility for which structural hazard may thus occur. Note: You are required to list five different and independent possibilities. I require so since for every possibility, it is implied that two stages are involved, and I do not want you to double-count that possibility.
3. (12%) We now look at control dependencies and hazards. Use the pipeline stages and what they do as stated in Appendix A.3 (reminder: Let the branch condition be resolved and target address be calculated in the stage AFTER the register-read stage).
 - (a) (3%) For a taken conditional branch, how many pipeline cycles must a plain pipeline waste in order to handle it? Give detailed enough explanation.
 - (b) (5%) With dynamic branch prediction, at best how many pipeline cycles must a plain pipeline waste in order to handle a taken conditional branch? Support your answer (indicate any required ISA features, data structures, hardware, and processing including its timing in your answer). The completeness determines your score, although it is only worth 5%.
 - (c) (4%) Explain the term “correlating branch predictors,” including how it is represented mathematically and how many predictors there will be.
4. (10%) Tomasulo’s Algorithm deserves particular attention for its capabilities in exposing ILP.
 - (a) What are all the major potential advantages this method can provide? (I can think of 3 or 4.) Give brief explanations.
 - (b) Using the five basic pipeline stages to begin with, now the pipeline should contain what stages? List the pipe stage names in order. (Listing only the names are fine, but use the commonly used names, or I may not know what you mean.) And between adjacent stages, where can there be stall cycles?

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1. (9%) Describe the characteristics, one main advantage, and one main disadvantage for each of the following three multithreading approaches: *fine-grained multithreading*, *coarse-grained multithreading*, and *simultaneous multithreading*.

2. (8%) Consider the following three processors:

- A simple MIPS 2-issue static pipe running at a clock rate of 4 GHz and achieving a pipeline CPI of 0.8. This processor has a cache system that yields 0.004 misses per instr.
- A deeply pipelined version of a 2-issue MIPS processor with slightly smaller caches and a 4 GHz clock rate. The pipeline CPI of the processor is 1.0, and the smaller cache yield 0.005 misses per instruction on average.
- A speculative superscalar with a 64-entry window. Its issue rate may achieve 4 instructions per clock. This processor has the smallest cache, which lead to 0.008 misses per instruction, but it hides 25% of the miss penalty on every miss by dynamic scheduling. This processor has a 2 GHz clock.

Assume that the main memory time is 50 ns. Determine the *miss penalty* in clock cycles, *CPI* (cycles per instruction), and *instruction execution rate* in MIPS (million instructions per second) for each processor. Which one of the three processors is best in performance, and which one is worst?

3. (6%) For each of the three **block placement** approaches, *direct mapped*, *set associative*, and *fully associative*, draw its address division diagram by showing the number of bit of each filed. Assume that the CPU address is N bits and byte addressable, the cache has 2^i blocks, the block size is 2^j bytes, and the cache has 2^k ways if it is set-associative. An exemplar address division diagram is given below.

Block address		Block offset
Tag	Index	

4. (7%) Answer the following four memory hierarchy questions for virtual memory.

- (a) Where can a block be placed in main memory? Why?
- (b) How is a block found if it is in the main memory of a paged virtual memory system?
- (c) Which block should be replaced on a virtual memory miss? Why?
- (d) What strategy should be applied on a write? Why?

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5. (10%) Typically, miss rate, miss penalty, hit time, and bandwidth are the main factors to evaluate the performance of a cache memory. Describe the following cache optimizations: *multilevel cache*, *way-prediction cache*, *nonblocking cache*, *critical word first*, and *hardware prefetching*. For each of the techniques, indicate one of the performance factors may be improved by it.
6. (10%)
- (a) (6%) Describe the characteristics, one main advantage, and one main disadvantage of the following two classes of MIMD multiprocessors: *centralized shared-memory multiprocessor* and *distributed-memory multiprocessor*.
 - (b) (4%) Describe and compare the following two cache coherence protocols: *directory-based*, and *snooping*.

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