國立交通大學試題紙

九十七學年度第一次
博士班資格考

科目：計算機結構(A)　　日期：98 年 2 月 5 日　第 1 頁 共 3 頁

請"✓"明　✓不可看書　可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (12%) About performance.

(a) (08%) A 2-GHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts:

Instruction type	Frequency	Clock cycle count
Integer ALU ops	40%	1
Floating-point ops	15%	8
Loads & Stores	25%	1
Branches	20%	2

Assume that the total number of instructions executed is 4,000,000.

i. (04%) Determine the effective CPI (cycle per instruction) and execution time for this program.

ii. (04%) Assume that we design a hardware enhancement to reduce the CPI (cycle per instruction) of the floating-point operations to 4 and build an optimizing compiler to discard 40% of the load and store instructions from the original instruction mix. Determine the effective CPI, execution time, and speedup of the enhancement.

(b) (04%) A common transformation required in graphics processors is square root. Suppose floating-point square root (FPSQR) is responsible for 40% of a critical graphics benchmark. One proposal is to enhance the FPSQR hardware and speed up this operation by a factor of 10. The other alternative is to make all floating-point (FP) instructions in the graphics processor run faster by a factor of 2; FP instructions are responsible for 80% of the execution time for the application. Compare these two design alternatives by evaluating the speedup of each proposal with respect to the original design. (4%)

2. (8%) For an arithmetic expression X = A + B – C, write the code sequence for each of the following four instruction set architecture classes: *stack*, *accumulator*, *register-memory*, and *register-register* (also called *load-store*). Assume that A, B, C, and X are belong in memory and that the values of A, B, and C cannot be destroyed. Moreover, assume that at most one memory operand is allowed in each of the arithmetic instructions of the register-memory architecture.

3. (10%) The cache optimizations may be classified into five categories: i. *reducing the hit time*, ii. *increasing cache bandwidth*, iii. *reducing the miss penalty*, iv. *reducing the miss rate*, and v. *reducing the miss penalty or miss rate via parallelism*. Describe the following cache optimizations and classified each of them according to the categories (i. ~ v.):
   (a) Critical word first (b) Trace cache (c) Hardware prefetching
   (d) Way prediction (e) Nonblocking cache

4. (8%) For a paged virtual memory system,
   (a) (02%) Where a block can be placed in main memory? Why?
   (b) (02%) How a block is found if it is in main memory?
   (c) (02%) Which block should be replaced on a virtual memory miss? How?
   (d) (02%) What happens on a write? Why?

5. (6%) Define the three classes of pipeline hazards and describe one possible way to reduce the stalls for each of them.

6. (6%) For a deep pipeline, it takes three pipeline stages before the branch-target address is known and an additional cycle before the branch condition is evaluated, assuming no stalls on the registers in the conditional comparison.
   (a) (03%) For three different branch prediction schemes (flushing pipeline, predicted taken, and predicted untaken), determine the branch penalties for each of the schemes when the pipeline encounters (i) an unconditional branch, (ii) a taken conditional branch, and (iii) a non-taken conditional branch.
   (b) (03%) Find the effective addition to the CPI arising from branches of this pipeline for each of the three prediction schemes, assuming the following frequencies:
      Unconditional branch: 3%
      Conditional branch, untaken: 6%
      Conditional branch, taken: 12%

7. (14%) About loop unrolling.
   (a) (04%) Explain it.
   (b) (10%) Explain three different types of limits to the gains that can be achieved by loop unrolling.

8. (14%) About Tomasulo's algorithm.
   (a) (04%) What is the purpose of this algorithm?
   (b) (10%) Draw the basic structure of a MIPS floating-point unit using the algorithm and explain functions of reservation stations and common data bus.

9. (08%) What are differences among superscalar, coarse multithreading, fine multithreading, and simultaneous multithreading?

10. (14%) About directory-based cache coherence protocol.
    (a) (04%) Explain it.
    (b) (10%) Draw its state transition diagram for an individual cache block and give explanations.