國 立 交 通 大 學 試 題 紙

一百零五學年度第二次
博士班資格考

科目：計算機架構 A

日期：106 年 7 月 26 日　第 1 頁 共 1 頁

請"✓"明　✓不可看書　可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (10%) We talk about ISAs:
   (a) (2%) The textbook points out that their most basic differentiation is *type of internal storage in processor*. Based on this, list the possible (four) ISA classes.
   (b) (8%) In addition, assuming we want to perform "D=E-F*G" on each of these classes, where D, E, F, and G are the operands' memory addresses, and E, F, and G cannot be destroyed. Show appropriate codes for each of these classes.

2. (10%) For addressing modes used by ISAs,
   (a) (6%) RISCs usually have only a small number of addressing modes. Explain why it is so. Also, indicate if there are limitations or requirements imposed on the selection of addressing modes, and explain why there should be such limitations/requirements.
   (b) (2%) How many addressing modes are used by the following MIPS-like instruction? Point out each individually, with sufficient explanations：

   Ld $s1, #8($a2)

   (c) (2%) Direct addressing mode is a very straightforward, powerful, and useful addressing mode. However, MIPS does not include this. Indicate what MIPS includes as it's alternative, and explain why MIPS does this, and how it actually works.

3. (10%) We study instruction format and control flow instruction relationships in MIPS.
   (a) (3%) Conditional branch instructions include only *BEQ* and *BNE*. Why is that? And what is wrong with the other kinds of conditional branch instructions?
   (b) (3%) *J* instruction is designed to be unconditional. Why is this? What advantage(s) will this bring us?
   (c) (4%) A subroutine call instruction is also included in MIPS instruction set. What is it? And compared with its sibling instruction "J", what extra work is involved in executing it? Will this instruction take longer to execute than "J"?

4. (10%) We study Tomasulo's algorithm in this problem:
   (a) (3%) What problem(s) does it intend to deal with? List only the name(s) with its meanings.
   (b) (4%) How does it deal with this problem(s)? Now you need to be specific and detailed, and use diagrams to help explain your idea if this can better make me understand what you mean.
   (c) (3%) This algorithm creates a serious architectural bottleneck. What is it? Why is it a bottleneck? And what can we do to alleviate this bottleneck? If so, are there concerns?

5. (10%) RISC ISAs have a number of features compared with CISC ISAs.
   (a) (4%) List five or more of these features.
   (b) (2%) All these features are for one clear goal. What is this goal? (There can be different answers; you may answer this question in your own view, and support your view.)
   (c) (4%) Now explain why these features can help better realize this goal(s), one at a time, clearly. Make sure that I can understand you, and agree to your opinions.

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命題老師簽名：

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一百零五學年度第二次
博士班資格考

科目：計算機架構 B

日期：106 年 7 月 26 日 第 1 頁 共 2 頁

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1. (12%)
   (a) (3%) What are the three key characteristics upon which the performance of a processor is dependent? List one of the three performance characteristics which will be affected by each of the following technologies: hardware organization, instruction set architecture, and compiler technology.
   (b) (9%) A 4-GHz processor was used to execute a benchmark program with the instruction mix and clock cycle counts shown in the table.

Instruction type	Frequency	CPI
Integer ALU ops	40%	1
Floating-point ops	15%	20
Loads & Stores	25%	4
Branches	20%	2

   i. Assume that the total number of instructions executed is 2×10^9.
   Determine the *effective CPI*, and *execution time* of this program.
   ii. Assume that we build an optimizing compiler to reduce 40% of the Load/Store operations from the original instruction mix. Determine the *effective CPI* of the enhancement and the *speedup* of the enhancement to the original design.
   iii. Determine the *percentage* of total execution time for floating-point instructions in the original design. If an enhancement with speedup equals to 5 is usable for these (floating-point) instructions, evaluate the *speedup* of the enhancement to the original design by Amdahl's Law.

2. (8%)
   (a) (4%) Define the following two main measures of dependability: *module reliability* and *module availability*.
   (b) (4%) For a disk subsystem with the components and MTTF (mean time to failure) as shown in the following table, assume that the lifetimes of the components are exponentially distributed, the failures are independent, and the average repair time of the components is 40 hours.

Component	No. of Components	MTTF (hours)
Disk	10	200,000
SCSI controller	2	40,000
Power supply	1	20,000
Fan	1	10,000

   Compute the *failure rate* in failures per hour of operation, the *reliability*, and the *availability* of the system.

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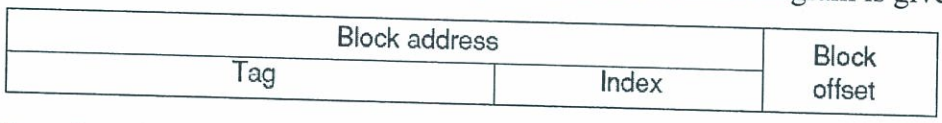
3. (14%)

(a) (6%) Describe the following three block placement approaches: ***direct mapped***, ***set associative***, and ***fully associative***. And draw the address division diagram by showing the number of bit of each filed for each of the approaches. Assume that the CPU address is N bits and byte addressable, the cache has 2^i blocks, the block size is 2^j bytes, and the cache has 2^k ways if it is set-associative. An exemplar address division diagram is given below.



(b) (8%) Describe the following cache optimizations: *way-prediction cache*, *nonblocking cache*, *merge write buffer*, and *hardware prefetching*. Moreover, indicate which of the following factors may be improved by each of the optimizations: *hit time*, *bandwidth*, *miss penalty*, *miss rate*, and *power consumption*.

4. (16%)

(a) (2%) Describe the advantages of SIMD (single instruction, multiple data) architecture versus MIMD (multiple instructions, multiple data) architecture.

(b) (6%) Describe the following three variations of SIMD: ***vector architectures***, ***multimedia SIMD instruction set extensions***, and ***graphics processing units*** (***GPUs***).

(c) (8%) Describe each of the following optimizations of vector architecture and indicate the problem solved by it:

i. Multiple lanes
ii. Vector-length register
iii. Vector mask register
iii. Stride

Hint: Possible problems solved:
① Handling multidimensional arrays
② Supplying bandwidth for vector load/store units
③ Beyond 1 element per clock cycle
④ Handling IF statements in vector loops
⑤ Handling sparse matrices
⑥ Handling loops not equal to the length of the vector register

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