

科目：計算機架構 A

日期：105 年 7 月 27 日 第 1 頁 共 2 頁

請“✓”明 ✓不可看書 可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (10%) There are five classes of computers based on their uses/environments. What are the five? And what are the critical system design issues of each of them? (Answer this problem using a table.)
2. (10%) In designing instruction set architecture (ISA) and computer system, there are several dramatically rapid changing implementation technologies that you should watch and predict closely.
 - (a) What are they?
 - (b) Use any one of your choice as an example, list its name, define it clearly, state why it is selected as being important, if it is really rapid changing, and why do you think that this rate of change will continue to be so.
3. (10%) Power reduction and energy efficiency have been stressed, especially in mobile devices. While energy efficient is very complex, we talk only about power here.
 - (a) What are the biggest problems in power design? (The answers can be various, although our textbook did specifically point out what they—three of them, are.)
 - (b) Explain when circuit will consume dynamic power.
 - (c) List dynamic power equation, and define each of the terms in the equation.
 - (d) Repeat (b) for static power.
 - (e) Repeat (c) for static power, again.
4. (10%) Among the six basic cache optimizations, one says “Avoiding address translation during indexing.”
 - (a) (2%) Which cache performance parameter does it intend to improve? Also explain.
 - (b) (3%) What does “address translation” mean? Be clear and specific.
 - (c) (2%) In the cache a virtual cache or a physical cache? Explain in detail.
 - (d) (3%) How large should the cache be? Again, be clear and specific.

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命題老師簽名：

國立交通大學試題紙

一百零四學年度第二次
博士班資格考

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5. (10%) Four kinds of parallelism are commonly known: Instruction, data, thread, and task parallelisms.
- (a) What type(s) of parallelism does the vector architecture intend to exploit or take advantage of?
How does the architecture exploit the type(s) of parallelism?
 - (b) Repeat (a) for SIMD architecture.
 - (c) Repeat (a) again for GPU (graphical processing unit).

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答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (9%) Describe the main feature, advantage, and disadvantage for each of the following instruction set architectures: *stack*, *accumulator*, and *load-store* architectures.
2. (10%) Give the equation to calculate the CPI (clocks per instruction) for a pipelined processor,
$$\text{Pipeline CPI} = \text{Ideal pipeline CPI} + \text{Structural stalls} + \text{Data hazard stalls} + \text{Control stalls}$$
For each of the following techniques, describe its basic idea and indicate which ones of the components of the CPI equation given above does the technique affect? If a technique affects data hazard stalls, please specify the dependence types (true, anti, and/or output dependences) of the hazards.
 - (a) Forwarding and bypassing
 - (b) Delayed branches
 - (c) Dynamic scheduling with renaming
 - (d) Function unit pipelining
 - (e) Loop unrolling
3. (5%) For a computer implemented in single-cycle implementation, assume that it has a clock cycle time of 12 ns. Design the computer as a traditional 5-stage pipelined implementation. After the stages are split by functionality, the measured times were IF, 2 ns; ID, 2.5 ns; EX, 2 ns; MEM, 3 ns; and WB, 2.5 ns. The pipeline register delay is 0.2 ns.
 - (a) (1%) What is the clock cycle time of the 5-stage pipelined machine?
 - (b) (2%) If there is a stall due to a data hazard every 4 instructions, what are the CPI of the new machine and the speedup of the pipelined machine over the single cycle machine?
 - (c) (2%) Assume that branches constitute 25% of the instructions, and the branch misprediction rate for the 5-stage pipelined machine is 20% and the misprediction penalty is 3 cycles. Calculate the CPI of the 5-stage machine and the speedup of the machine over the single cycle machine, taking into account not only the stalls due to data hazards described in (b) but also the stalls due to branch mispredictions.

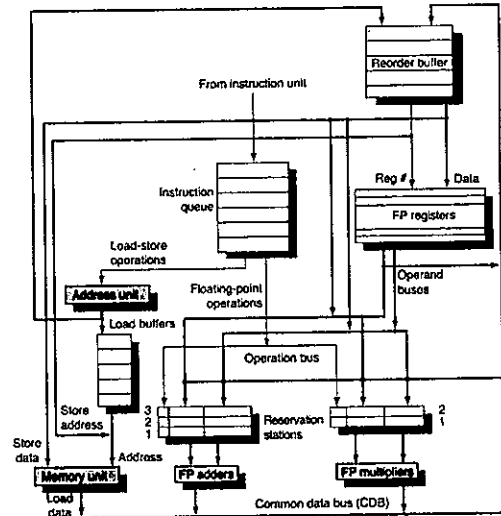
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4. (8%) Given the structure of **Tomasulo algorithm with reorder buffer (ROB)**, describe the key idea of this Tomasulo algorithm, the main purposes of using reservation stations and ROB in this structure, and the following four steps involved in instruction execution: *Issue, Execute, Write result, Commit*.



5. (6%) Describe the characteristics, one main advantage, and one main disadvantage for each of the following multithreading approaches: *fine-grained*, *coarse-grained*, and *simultaneous multithreading*.
6. (12%)
- (a) (6%) Draw the block diagram of the basic structure for each of the following two classes of MIMD (multiple instruction stream, multiple data stream) multiprocessors and describe the characteristics, one main advantage, and one main disadvantage for each of them: *centralized shared-memory multiprocessor* and *distributed shared-memory multiprocessor*.
- (b) (6%) Describe and compare the following two cache coherence protocols: *snooping* and *directory-based*.