國 立 交 通 大 學 試 題 紙

一百學年度第二次
博士班資格考

科目：計算機結構(A)　　日期：101 年 7 月 25 日　第 1 頁 共 1 頁

請" ✓" 明　　✓不可看書　　可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. **(30 points)** Based on Flynn's classification, processor architectures can be divided into SISD, SIMD, MISD, and MIMD categories.
   (a) (4pts) Explain what those categories stand for.
   (b) (4pts) Conventional single-processor von Neumann computers are classified as SISD systems. Explain what "von Neumann bottleneck" is?
   (c) (4pts) What is the key idea of SIMD? Explain why vector processors are SIMD.
   (d) (5pts) Contemporary GPU (Graphic processing unit) is another SIMD example. Give at least three key features in GPU.
   (e) (7pts) Show and explain the key differences between SIMD and MIMD by drawing simple architectures.
   (f) (6pts) For the following architectures, classify each of the following to which of the above categories.
   (1) Pipelined RISC (2) MMX/SSE streaming (3) multicore
   (4) multiprocessor (5) distributed systems (6) VLIW.

2. **(20 points)** Assume the main memory access time is 200ns. Consider the following three processors.
   [A] A simple 5-stage RISC pipeline with a clock rate of 500 MHz and a pipeline CPI of 1.1. This processor has a cache system that yields 0.03 misses per instruction.
   [B] A deeply pipelined version of the same RISC with slightly smaller caches and a 800 MHz clock rate. The pipeline CPI of this processor is 1.5, and the smaller caches yield 0.04 misses per instruction on average.
   [C] A 4-issue superscalar machine with 32-entry instruction window and sufficiently large reorder buffer. It achieves 75% of the ideal issue rate. (The idea amount of parallelism available is 4.) This processor has the smallest caches which leads to 0.055 misses per instruction. This processor has a 400 MHz clock.

   (a) (6pts) Determine the relative timing performance of these three processors for executing M instructions.
   (b) (4pts) Make comments on how the architectural differences of these three CPUs contribute to their clock rates and CPI.
   (c) (6pts) Give the design complexity and compare the overall cost (in terms of issues such as area and power) to achieve performance.
   (d) (4pts) How would you make your own new choice? Why?

◎請用深黑色鋼筆或原子筆出題

命題老師簽名：

國 立 交 通 大 學 試 題 紙

一百學年度第二次
博士班資格考

科目:計算機結構(B)　　日期: 101 年 7 月 25 日　第 1 頁 共 2 頁

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答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (6%)
   (a) In our textbook, what does "memory wall" mean?
   (b) What problems this "wall" will cause?
   (c) And how are these problems usually handled?

2. (9%)
   (a) What does "load-store architecture" mean in instruction-set architecture design?
   (b) Does RISC adopt this design guideline? Why or why not?
   (c) Repeat (b) but this time for CISC.

3. (11%) RISCs somehow depend on having a large general-purpose register file to gain performance.
   (a) (3%) Why is this, and how large is considered large?
   (b) (3%) What is good if these registers are general-purpose?
   (c) (5%) With Moore's law, is the register file the bigger the better? List the yeses and no's that you can think of, with necessary explanations.

4. (12%) Let there be two private caches $0 and $1 in a snoopy system. The states of a cache line can be [*invalid, shared, exclusive*]. Let the cache write policy be write-back.
   (a) (2%) What are the differences between states *shared* and *exclusive*? (Be complete in answering this question.)
   (b) (10%) Let the caches be initially empty, and perform the following operations in order:
   Time0--$0 reads LineA;
   Time1--$0 reads LineB;
   Time2--$1 reads LineA;
   Time3--$0 writes LineA;
   Time4--$1 reads LineA;
   Time5--$1 writes LineB;
   Time6--$1 writes LineA.

   Complete the following table as much as you can ("Necessary bus control signals issued" should contain typical and snooper signals):

Instance	$0 Line states	$1 Line states	If miss, how to obtain line	Necessary bus control signals issued
End of Time0	A: B:	A: B:		

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End of Time1	A: B:	A: B:		
End of Time2	A: B:	A: B:		
End of Time3	A: B:	A: B:		
End of Time4	A: B:	A: B:		
End of Time5	A: B:	A: B:		
End of Time5	A: B:	A: B:		

5. (12%) In original IBM 360/91 Tomasulo's algorithm, let there be F floating-point registers, A adder reservation stations, M multiplier reservation stations, L load buffer entries, and S store buffer entries.
   (a) List the purposes this design intends to satisfy.
   (b) What is the performance bottleneck of this design?
   (c) How many effective registers can you see at most?
   (d) A very serious problem is caused in this design; in some situation, this problem can even be called a mistake. What is it?