

科目：計算機架構 A

日期：104 年 1 月 26 日 第 1 頁 共 2 頁

請“✓”明 ✓不可看書 可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (10%) We talk about ILP (instruction-level parallelism) and its limitations here. Answer the following questions concisely but to the points:
 - (a) (3%) Why register renaming can help ILP? That is, what problems does it intend to eliminate, and what benefit(s) can be gained?
 - (b) (3%) Why branch prediction can help ILP? That is, what problems does it intend to eliminate, and what benefit(s) can be gained?
 - (c) (2%) Does branch prediction require the use of instruction window? Why or why not?
 - (d) (2%) Instruction window can serve many purposes. Pick one of the purposes that you think is very important, and explain how it fulfills that purpose.
2. (9%) Let us talk about MIMD.
 - (a) (3%) When we say shared-memory multiprocessors (SMPs), what indeed do these processors share? I know it says the memory, but be very specific: What type of memory? Describe this memory to the points.
 - (b) (3%) Then we may further say the multiprocessor architecture is of the UMA (uniform memory access) type. What do we mean by UMA? Include all necessary features in your answer, and better itemize them.
 - (c) (3%) Then we may also sometimes say the multiprocessors are symmetric. What do we mean here? Again, include all necessary features in your answer, and better itemize them.
3. (4%) For a shared-memory multiprocessor, you need to understand why caches can be incoherent, and how this problem should be dealt with. Give an example showing why caches can be incoherent. Your answer should include: A multiprocessor's system block diagram, and a running code example in stepwise fashion showing why cache incoherence will occur.
4. (12%) In memory hierarchy design,
 - (a) (4%) What are the popular hierarchies in a desk-top computer system?
 - (b) (4%) For each of the hierarchies in your Part (a) answer, what is using (or controlling the use of) that hierarchy? (There can be different answers, but I want you to give me the most realistic and popular answers.)
 - (c) (4%) What are the four common questions for a higher level of the memory hierarchy?
5. (5%) For a cache of fixed capacity, going from direct-mapped to fully associatively mapped, how many more tag bits will be needed? (Although this is a very fundamental question, you need to assume some variables in order to answer to it.)

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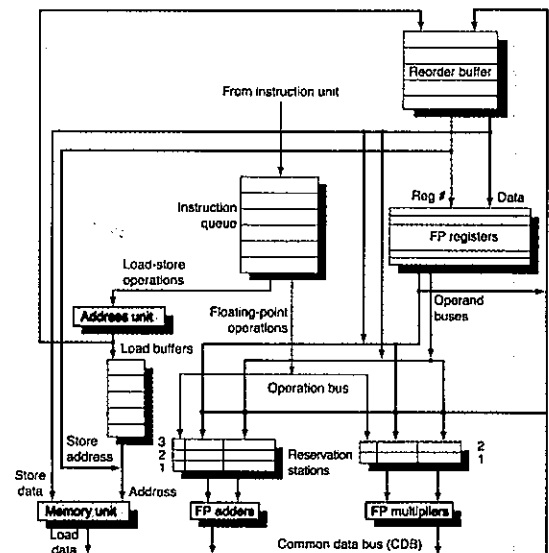
4. (10%) Give the equation to calculate the value of the CPI (clocks per instruction) for a pipelined processor:

Pipeline CPI = Ideal pipeline CPI + Structural stalls + Data hazard stalls + Control stalls

For each of the following techniques, describe the technique briefly and indicate the components of the CPI equation affected by the technique. If a technique affects data hazard stalls, please specify the dependence types (true, anti, and/or output dependences) of the hazards.

- Forwarding and bypassing
- Dynamic scheduling with renaming
- Issuing multiple instructions per cycle
- Hardware speculation
- Delay branches

5. (10%) Given the structures of Tomasulo algorithm with reorder buffer (ROB) to handle speculation,
- (2%) Describe two key ideas of this Tomasulo algorithm.
 - (8%) Describe the following four stages of the algorithm: Issue, Execute, Write result, Commit.



6. (6%) Describe the characteristics, one major advantage, and one major disadvantage for each of a VLIW (very long instruction word) processor and a dynamically scheduled superscalar processor.

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1. (10%)

- (a) (4%) Define the following two main measures of dependability: *module reliability* and *module availability*. (4%)
- (b) (6%) Describe the following schemes of dynamic branch prediction: 1-bit prediction, 2-bit prediction, and correlating branch prediction.

2. (8%)

- (a) (4%) A 2-GHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts:

Instruction type	Frequency	Clock cycle count
Integer ALU ops	40%	1
Floating-point ops	20%	10
Loads & Stores	30%	3
Branches	10%	2

Assume that the total number of instructions executed is 4,000,000, determine the effective CPI and execution time for this program.

- (b) (4%) Assume that we have accomplished two enhancements. One is to reduce the CPI of the FP operations to 8 and another is to discard one-third of the load/store instructions from the original instruction mix. Determine the effective CPI after the enhancements and the speedup to the original design.

3. (6%) Describe the goal of loop unrolling and four of the major decisions or transformations made for obtaining the final unrolled code of a loop.

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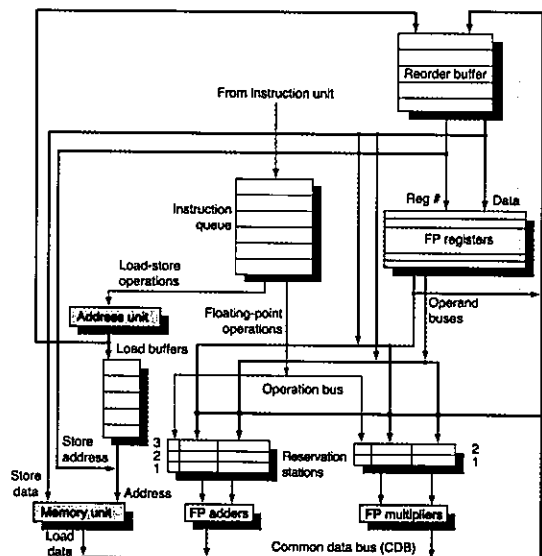
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