國 立 交 通 大 學 試 題 紙

一百零三學年度第二次
博士班資格考

科目:計算機架構 A　　日期: 104 年 7 月 29 日　第 1 頁 共 2 頁

請" ✓" 明　　✓不可看書　　可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. In designing processors with very high ILP (instruction-level parallelism), we often also incorporate multithreading.
   (a) (4%) Why would we like to do this? That is, is there something wrong if we do not do this?
   (b) (6%) How many types of multithreading does the textbook introduce? Brief explain each.
   (c) (4%) Which of these typically has the best result, and why? In showing this, do not forget to compare your chosen type with the others.

2. We have two classes of MIMD multiprocessors: Centralized shared-memory architectures, and distributed-memory architectures.
   (a) (4%) Define the terms UMA and NUMA. Then, which class is UMA type, and which is NUMA.
   (b) (3%) List the advantages and disadvantages of UMA multiprocessors.
   (c) (3%) Repeat (b) for NUMA multiprocessors.

3. In broadcast- (or bus-) based cache coherence protocols,
   (a) (2%) Are they called Snoopy, or Directory protocols? Why?
   (b) (4%) List all local processor-cache activities that can cause other caches to react, and explain how other caches should react.
   (c) (3%) Compared with the other possibility, what advantages does this type of protocols have?
   (d) (3%) Continued from (c), what problems does this type of protocols have? And has the other type corrected these problems? If yes, how?

◎ 請用深黑色鋼筆或原子筆出題

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4. (14%) Assume a pipelined computer system with the following features:
   1. CPI (Cycles-per-instruction) is 1 if not memory access instructions and assume an ideal memory;
   2. Half of the instructions executed are memory access instructions;
   3. Main memory access time and cycle time are both 100 cycles;
   4. All cycles mentioned in this problem are CPU clock cycles.

   Then what is the average instruction execution rate (in number of cycles per instruction) given that:

   (a) (2%) If there is no cache memory?

   (b) (4%) If there is only one cache, with hit time of three cycles and miss rate of 10%?

   (c) (4%) If there are two split caches, with the same specifications as above?

   (d) (4%) If there are two split caches, each with hit time of one cycle and miss rate of 30%, and a lower-level cache with hit time of 5 cycles and miss rate of 10%?

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科目:計算機架構 B　　日期: 104 年 7 月 29 日　第 1 頁 共 2 頁

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1. (20%) For each statement given below, determine whether it is correct (**True**, **T**) or not (**False**, **F**) and describe your reasons. (Score is given only if the reason expressed by you is correct.)
   (a) MIPS (Millions Instructions Per Second) is a good metric to measure computer performance.
   (b) When we use performance ratios, e.g., SPECRatios, to make comparisons, use the geometric mean instead of arithmetic mean to summarize the performance results.
   (c) For CMOS chips, the dynamic power required per transistor is proportional to the voltage.
   (d) Module availability is a measure of the continuous service accomplishment from a reference initial instant. Therefore, the mean time to failure is an availability measure.
   (e) The goal of pipeline is to improve instruction throughput rather than individual instruction execution time.
   (f) The pipeline registers carry data only from one pipeline stage to the next.
   (g) Page fault is a synchronous, coerced, maskable, within instructions, terminated exception.
   (h) When extending the typical 5-stage MIPS pipeline to handle multicycle operations, WAW and WAR hazards are possible.
   (i) In computers that allow misaligned memory access, misaligned accesses are usually executed faster than aligned accesses.
   (j) For a (3, 2) correlation predictor indexed by the lower eight bits of the address of the branch instruction, 2048 bits are required in the branch prediction buffer.

2. (8%) Assume a disk subsystem with the components and MTTF (mean time to failure) as shown in the table. The lifetimes of the components are exponentially distributed and the failures are independent.

Component	No. of Components	MTTF (hours)
Disk	8	100,000
SCSI controller	1	50,000
Power supply	1	20,000
Fan	1	10,000

   (a) Compute the failure rate in failures per hour of operation, the reliability, and the availability of the system. Assume that the average repair time of the components is 40 hours.
   (b) Assume that one fan is sufficient to run the disk subsystem, one redundant fan is added to the subsystem, and the repair time of a fan is 20 hours. Calculate the reliability of the fan pair, evaluate how much is the fan pair more reliable than a single fan, and determine the reliability improvement of the system due to the fan pair by Amdahl's Law.

3. (6%) Describe the advantages and disadvantages for each of the *stack*, *accumulator*, and *general-purpose-register* architectures.

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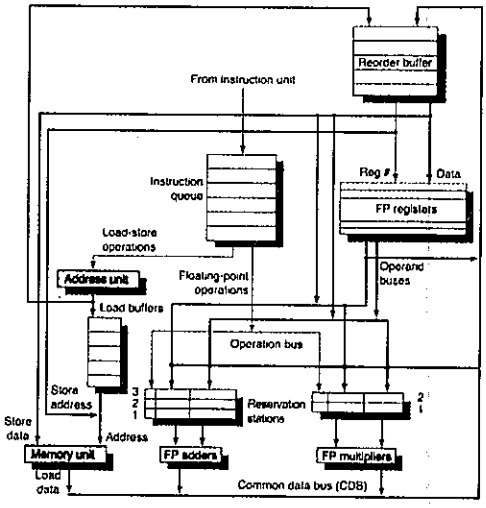
4. (6%) For each of the following techniques, describe the technique briefly and indicate which ones of the factors, including *ideal pipeline CPI*, *structural stalls*, *data hazard stalls*, and *control stalls*, for evaluating the CPI (clocks per instruction) of a pipelined processor are affected by the technique. If a technique affects data hazard stalls, please specify the dependence types (true, anti, and/or output dependences) of the hazards.
   (a) Forwarding and bypassing　(b) Superscalar with speculation　(c) Loop unrolling

5. (10%) Given the structure of Tomasulo algorithm with reorder buffer (ROB),
   (a) (3%) Describe the key idea of this Tomasulo algorithm and the main purposes of using reservation stations and ROB in this structure.
   (b) (3%) Describe the *commit* step involved in executing each of the *arithmetic*, *load*, *store*, and *branch* instructions.
   (c) (4%) Consider the execution of the following code on this single-issue Tomasulo MIPS pipeline. An FP register is denoted as Fi and an integer register as Ri.




```
1  L.D     F0, 0(R1)   ;load double word into F0
2  MUL.D   F4, F2, F0  ;F4 = F2 × F0
3  SUB.D   F2, F0, F6  ;F2 = F0 – F6
4  ADD.D   F2, F2, F4  ;F2 = F2 + F4
5  S.D     F2, 0(R1)   ;store F2 into memory
```

   Make the following assumptions:
   - The EX cycle latencies for FP functional units:
     Add/Subtract: 2 cycles;
     Multiply: 4 cycles;
     Divide: 8 cycles
   - There are two FP adder (+/–), two FP multipliers (×/÷), and one integer unit.
   - There are two read ports and one write port for the register file.
   - There are two reservation stations for each of the FP adders and multipliers.
   - Only one CDB exists in the processor.

   Show the clock cycle number for each step of the instructions in the code sequence. Express your answer as the following table:

Instruction		Issue	Operand ready	Execution complete	Write result to CDB	Commit
L.D	F0, 0(R1)	1	2	3	4	5
MUL.D	F4, F2, F0					
SUB.D	F2, F0, F6					
ADD.D	F2, F2, F4					
S.D	F2, 0(R1)					